**Tutorial's title:** Design for Excellence Practices for Integrated Circuits

**Tutorial type:** Introductory to intermediate

**Summary:** The semiconductor supply chain encompasses a web of multiple companies designing, manufacturing, testing, packaging, and distributing semiconductors, often dispersed globally. This mode of the supply chain requires the application of good Design for Excellence (DFX) practices to ensure manufacturability, quality, and profitability. This introductory to intermediate-level tutorial will present an overview of the design stages and tasks for a fabless IC design cycle. It will describe all the key methodologies and techniques used in each task, such as Design for testing, debugging, diagnostics, and manufacturability. What DFX techniques and trade-offs are applicable for each technique, and what return on investment do they bring in cost, quality, yield, and reliability for the high-volume manufactured chips? The DFX techniques for new areas like chips for Artificial Intelligence (AI), data centers, open-source processors, and multi-die packaging and integrated systems will be highlighted in the tutorial.

This tutorial will be highly relevant to the 1st IEEE International Conference on Design, Test, and Technology of Integrated Systems (DTTIS) participants, as it ties all design, test, integration, and manufacturing aspects. The tutorial will appeal to design, test, CAD, and yield engineers and students pursuing careers in these fields as well as the managers and executives of the semiconductor industry.

**Detailed Outline**

1. IC Design Cycle: Overview of all the design steps from architecture to implementation of a cell-based design cycle, RTL, Verification, Synthesis, Layout and Planning, Timing Analysis, and Tapeout.
2. Fabless Design and Manufacturing Process, supply chain ecosystem for fabless manufacturing.
3. Design for Excellence, Cost, and Yield: The basic relationship between cost, area, design, yield, and testing.
4. Design for Test; Scan, Boundary Scan, Logic and Memory BIST, and ATPG.
5. Design for Debug: IJTAG and other ad-hoc methods.
6. Design for Diagnostics: Logic and Memory Diagnostics.
7. Design for Manufacturability: Process monitors, IR drop analysis, Reliability, Hot spot stimulation.
8. Yield Analysis and Management Systems: Yield Analysis, Root Cause, and Failure Analysis.

**About the presenter:** Saghir A. Shaikh, Ph.D., works as a DFX Technologist at Intel Corporation, San Diego, CA. He has 25 years of design and test implementation experience with companies such as Level One Communications, Sun Microsystems, Cadence Design Systems, and Broadcom Corp. Dr. Shaikh is the Senior Member of the IEEE and Member of IEEE's Test Technology Standards Committee. He has (co)authored more than two dozen papers presented at conferences and published in magazines and journals. He has been on program and paper review committees of several IEEE Conferences.

Dr. Shaikh has 20 years of experience presenting and tutoring at IEEE-sponsored events such as International Test Conferences, VLSI Test Symposiums, Asian Test Symposiums, and Latin American Test Workshop. His tutorials on Mixed-Signal and RF Testing had the most registrations for multiple years and received, on average, 4.3/5.0 overall ranking in all his tutorials. In addition, Dr. Shaikh regularly presented and mentored engineers and managers at his workplace. Dr. Shaikh also has extensive public speaking experience at community-related events on non-technical topics.

**Duration of the Tutorial:** 90 minutes – 180 minutes.

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